AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing of claims in the application:

Claim 1 (Currently amended): A method of transforming a first topology to a reduced topology, said first topology representing an abstraction of one or more objects, said first topology further comprising a plurality of inter-connected elements, said method comprising [[the steps of]]:

[[(a)]] identifying one or more elements, wherein the identifying comprises generating a minimum spanning tree (MST) of the first topology and identifying one or more small-valued circuit elements in the MST;

[[(b)]] analyzing [[the]] an effect of reducing one or more of said identified elements on [[the]] topological and physical characteristics of said one or more objects[[, and]], wherein the analyzing comprises analyzing a variation of one or more delay measurements after eliminating one or more of said small-valued circuit elements;

~~(c)if the effect is negligible,~~ generating a second topology reflecting [[the]] a reduction of one or more identified elements in response to the effect of reducing one or more of said identified elements has negligible effect on the topological and physical characteristics of said one or more objects, wherein the reducing one or more said identified elements comprises eliminating one or more of said small-valued circuit elements in the MST.

Claim 2 (Currently amended): The method of claim 1, further comprising [[the step of]]

(d) recursively executing ~~steps (a)-(c)~~ the identifying, the analyzing, and the generating processes until no further reduction is possible.

Claim 3 (original): The method of claim 2, wherein the second topology is a reduced topology.

Claim 4 (Canceled).

Claim 5 (Canceled).

Claim 6 (Currently amended): The method of claim 1, wherein [[step (a)]] the identifying further comprises [[the step of]]

identifying one or more symmetric nodes from a single input tree structure.

Claim 7 (Currently amended): The method of claim 6, wherein [[step (a)]] the identifying further comprises: [[the step of]]

identifying one or more symmetric nodes in a top-down fashion from the single input tree structure.

Claim 8 (Currently amended): A method of transforming a circuit from a first topology to a reduced topology, said first topology comprising a plurality of inter-connected circuit elements, said method comprising [[the steps of]]:

[[(a)]] identifying one or more circuit elements having coupling effects;

[[(b)]] analyzing [[the]] an effect of reducing one or more of said identified circuit elements on [[the]] topological and physical characteristics of said circuit, wherein the analyzing comprises

producing a first regional topology approximating an effect of eliminating one or more circuit elements having coupling effect;

identifying one or more crossly-coupled nodes within the first regional topology;

estimating coupling effects of each said one or more crossly-coupled nodes; and

~~(c) if the effect satisfies a first predefined standard,~~ generating a second topology reflecting [[the]] a reduction of one or more identified circuit elements in response to the effect of reducing one or more of said identified circuit elements on the topological and physical characteristics of said circuit satisfies the first predefined standard, wherein the generating includes replacing cross-coupling of each crossly-coupled node with its estimated coupling effects.

Claim 9 (Currently amended): The method of claim 8, further comprising: [[the step of]]

(d) recursively executing ~~steps (a)-(c)~~ the identifying, the analyzing, and the generating processes until no further reduction is possible.

Claim 10 (Currently amended): The method of claim 9, further comprising [[the steps of]]:

[[(e)]] replacing the first predefined standard with a second predefined standard; and [[,]]

[[(f)]] repeating ~~steps (a)-(d)~~ the identifying, the analyzing, the generating, and the replacing processes for the reduced topology using the second predefined standard.

Claim 11 (original): The method of claim 10, wherein the second predefined standard is a more relaxed standard than the first predefined standard.

Claim 12 (Currently amended): The method of claim 8, wherein [[step (a)]] the identifying further comprises [[the step of]] producing a topological approximation of the first topology.

Claim 13 (original): The method of claim 12, wherein the topological approximation is a minimum spanning tree (MST).

Claim 14 (Currently amended): The method of claim 13, wherein [[step (a)]] the identifying further comprises [[the step of]] identifying one or more circuit elements from the MST, the value of each said one or more circuit elements is less than a threshold value.

Claim 15 (Currently amended): The method of claim 8, wherein [[step (b)]] the analyzing further comprises [[the step of]] analyzing [[the]] a variation of one or more delay measurements.

Claim 16 (original): The method of claim 15, wherein the one or more delay measurements comprise Elmore delays.

Claim 17 (Currently amended): The method of claim 14, wherein [[step (c)]] the generating further comprises [[the step of]] eliminating the one or more circuit elements whose value is less than a threshold value.

Claim 18 (Cancelled).

Claim 19 (Cancelled).

Claim 20 (Currently amended): The method of claim 8, wherein [[step (a)]] the identifying further comprises [[the step of]] identifying one or more clusters of circuit elements.

Claim 21 (Currently amended): The method of claim 20, wherein [[step (b)]] the analyzing further comprises [[the steps of]]

determining one or more center nodes for one or more clusters; and[[,]]

analyzing [[the]] an effect of moving the connection of one or more circuit elements connected to one or more nodes within one or more said clusters to one or more said center nodes.

Claim 22 (Currently amended): The method of claim 8, wherein [[step (a)]] the identifying further comprises [[the step of]]

identifying one or more circuit elements having similar input-output characteristics.

Claim 23 (Currently amended): The method of claim 22, wherein [[step (c)]] the generating further comprises [[the step of]]

merging one or more of said circuit elements having similar input-output characteristics into one equivalent circuit element.

Claim 24 (Currently amended): The method of claim 8, wherein [[step (a)]] the identifying further comprises [[the step of]]

identifying one or more candidate nodes including one or more quick nodes,

wherein said one or more candidates do not include any node having a capacitor directly connected to an input node.

Claim 25 (Currently amended): The method of claim 24, wherein [[step (c)]] the generating further comprises [[the step of]]

eliminating one or more candidate nodes only if its degree of connectivity is equal to two.

Claim 26 (Currently amended): The method of claim 24, wherein [[step (b)]] the analyzing further comprises [[the steps of]]:

producing a regional topology approximating [[the]] an effect of eliminating one or more of said candidate nodes; and,

determining, based on the regional topology, [[the]] a difference in [[the]] a number of circuit elements connected between two or more neighboring nodes of one or more of said candidate nodes, before and after eliminating one or more of said candidate nodes.

Claim 27 (Currently amended): The method of claim 26, wherein [[step (c)]] the generating further comprises [[the step of]]

eliminating one or more of said candidate [[notes]] nodes, if the regional topology produces less number of circuit elements connected between two or more neighboring nodes of one or more of said candidate nodes.

Claim 28 (Currently amended): The method of claim 24, wherein [[step (b)]] the analyzing further comprises [[the step of]]

determining if the topology after eliminating one or more of said candidate nodes contains a voltage divider structure.

Claim 29 (Currently amended): The method of claim 28, wherein [[step (c)]] the generating further comprises [[the step of]]

eliminating said one or more candidate nodes if the topology after eliminating one or more of said candidate nodes does not contain a voltage divider structure.

Claim 30 (Currently amended): The method of claim 8, wherein [[step (a)]] the identifying further comprises [[the step of]]

identifying a regional topology comprising two nodes N_1 and N_2 connected to a common node N_a, wherein N_1 is connected to N_a through resistance R_1, N_2 is connected to N_a through resistance R_2, N_1 and N_2 further having capacitance C_1 and C_2, respectively, connected to either the ground or another common node, and wherein there is no other resistor connection to N_1 or N_2.

Claim 31 (Currently amended): The method of claim 30, wherein [[step (c)]] the generating further comprises [[the step of]]

merging N_1 and N_2, if (i) the value of R_1*C_1 is approximately equal to the value of R_2*C_2, and (ii) if N_1 and N_2 are connected to additional common nodes N_{b1}, N_{b2},...,N_{bn} via capacitors C_{c11}, C_{c12}, ...C_{c1n} and C_{c21}, C_{c22}, ...C_{c2n}, respectively, the value of R_1*C_{c1i} is approximately equal to the value of R_2*C_{c2i}, for i=1...n.

Claim 32 (Currently amended): The method of claim 12, wherein [[step (a)]] the identifying further comprises [[the step of]]

identifying one or more symmetric nodes.

Claim 33 (Currently amended): The method of claim 32, wherein [[step (c)]] the generating further comprises [[the step of]]

merging said one or more symmetric nodes.

Claim 34 (original): The method of claim 8, wherein the plurality of circuit elements comprise resistors and capacitors.

Claim 35 (Currently amended): The method of claim [[18 or 19]] 8, wherein the one or more circuit elements having coupling effect comprise one or more coupling capacitors.

Claim 36 (original): The method of claim 21, wherein the one or more circuit elements connected to one or more nodes within one or more said clusters comprise one or more coupling capacitors.

Claim 37 (Currently amended): The method of claim 28 [[or 29]], wherein the voltage divider structure comprises two or more capacitors connected in series.

Claim 38 (Canceled).

Claim 39 (Currently amended): A programmed computer system for transforming a first topology to a reduced topology, said first topology representing an abstraction of one or more objects, said first topology further comprising a plurality of inter-connected elements, said

programmed computer system comprising at least one memory having at least one region storing computer executable program code and at least one processor for executing the program code stored in said memory, wherein the program code comprises:

[[(a)]] code to identify one or more elements, wherein the code to identify includes code to identify one or more clusters of circuit elements and code to determine one or more center nodes for one or more clusters;

[[(b)]] code to analyze [[the]] an effect of reducing one or more of said identified elements on [[the]] topological and physical characteristics of said one or more objects, wherein the code to analyze includes code to analyze effect of moving a connection of the one or more circuit elements connected to one or more nodes within the one or more clusters to the one or more center nodes; and

[[(c)]] code to generate a second topology reflecting [[the]] a reduction of one or more identified elements in response to reducing one or more of said identified elements has negligible effect on the topological and physical characteristics of said one or more objects, wherein the code to generate the second topology includes code to move the connection of the one or more circuit elements within the one or more clusters to the one or more center nodes.

Claim 40 (Currently amended): The system of claim 39, wherein the program code further comprises code to recursively executing ~~(a), (b) and (c)~~ the code to identify, the code to analyze, and the code to generate until no further reduction is possible.

Claim 41 (original): The system of claim 40, wherein the second topology is a reduced topology.

Claim 42 (original): The system of claim 39, wherein the program code further comprises code to produce a topological approximation of the first topology.

Claim 43 (original): The system of claim 42, wherein the topological approximation is a minimum spanning tree (MST).

Claim 44 (original): The system of claim 43, wherein the program code further comprises code to identify one or more symmetric nodes.

Claim 45 (original): The system of claim 44, wherein the program code further comprises code to identify one or more elements of small-value from the MST.

Claim 46 (original): The system of claim 39, wherein the plurality of inter-connected elements comprise a plurality of circuit elements.

Claim 47 (Currently amended): The system of claim 46, wherein the program code further comprises code to analyze [[the]] a variation of one or more delay measurements.

Claim 48 (original): The system of claim 46, wherein the program code further comprises code to identify one or more circuit elements having coupling effect.

Claim 49 (Currently amended): The system of claim 48, wherein the program code further comprises:

code to produce a first regional topology approximating [[the]] an effect of eliminating one or more circuit elements having coupling effect;

code to identify one or more crossly-coupled nodes within the first regional topology;

code to estimate [[the]] coupling effects of each said one or more crossly-coupled nodes; and

code to generate a second regional topology replacing [[the]] cross-coupling of each crossly-coupled node with its estimated coupling effects.

Claim 50 (Canceled).

Claim 51 (Canceled).

Claim 52 (original): The system of claim 46, wherein the program code further comprises code to identify one or more circuit elements having similar input-output characteristics.

Claim 53 (original): The system of claim 52, wherein the program code further comprises code to merge one or more of said circuit elements having similar input-output characteristics into one equivalent circuit element.

Claim 54 (original): The system of claim 46, wherein the program code further comprises code to identify one or more candidate nodes including one or more quick nodes,

wherein said one or more candidates do not include any node having a capacitor directly connected to an input node.

Claim 55 (original): The system of claim 54, wherein the program code further comprises code to eliminate one or more candidate nodes only if its degree of connectivity is equal to two.

Claim 56 (Currently amended): The system of claim 54, wherein the program code further comprises:

code to produce a regional topology approximating [[the]] an effect of eliminating one or more of said candidate nodes; and,

code to determine, based on the regional topology, [[the]] a difference in [[the]] a number of circuit elements connected between two or more neighboring nodes of one or more of said candidate nodes, before and after eliminating one or more of said candidate nodes.

Claim 57 (Currently amended): The system of claim 56, wherein the program code further comprises code to eliminate one or more of said candidate [[notes]] nodes, if the regional topology produces less number of circuit elements connected between two or more neighboring nodes of one or more of said candidate nodes.

Claim 58 (original): The system of claim 54, wherein the program code further comprises code to determine if the topology after eliminating one or more of said candidate nodes contains a voltage divider structure.

Claim 59 (original): The system of claim 58, wherein the program code further comprises code to eliminate said one or more candidate nodes if the topology after eliminating one or more of said candidate nodes does not contain a voltage divider structure.

Claim 60 (original): The system of claim 46, wherein the program code further comprises code to identify a regional topology comprising two nodes N_1 and N_2 connected to two common nodes N_a and N_b, wherein N_1 is connected to N_a through capacitance C_{c1} and to N_b through resistance R_1, N_2 is connected to N_a through capacitance C_{c2} and to N_b through resistance R_2, N_1 and N_2 further having ground capacitance C_1 and C_2, respectively.

Claim 61 (original): The system of claim 60, wherein the program code further comprises code to merge N_1 and N_2, if the value of R_1*C_1 is approximately equal to the value of R_2*C_2 and the value of R_1*C_{c1} is approximately equal to the value of R_2*C_{c2}.

Claim 62 (Canceled).

Claim 63 (Canceled).

Claim 64 (Canceled).

Claim 65 (Canceled).

Claim 66 (Canceled).

Claim 67 (Canceled).

Claim 68 (Canceled).

Claim 69 (Canceled).

Claim 70 (Currently amended): Computer executable software code stored on a computer readable medium for transforming a first topology to a reduced topology, said first topology representing an abstraction of one or more objects, said first topology further comprising a plurality of inter-connected elements, said software code comprises:

[[(a)]] code to identify one or more elements having similar input-output characteristics;

[[(b)]] code to analyze [[the]] an effect of reducing one or more of said identified elements on [[the]] topological and physical characteristics of said one or more objects, and

[[(c)]] code to generate a second topology reflecting [[the]] a reduction of one or more identified elements in response to reducing one or more of said identified elements has negligible effect on the topological and physical characteristics of said one or more objects ~~if the effect is negligible~~, wherein the code to generate includes code to merge one or more of said circuit elements having similar input-output characteristics into one equivalent circuit element.